



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

10/798,994

03/11/2004

Jeffery Steven Beck

10030326-1

6851

68551

7590

03/04/2009

RatnerPrestia

P.O. BOX 980

VALLEY FORGE, PA 19482

EXAMINER

NGUYEN, LUONG TRUNG

ART UNIT

PAPER NUMBER

2622

MAIL DATE

DELIVERY MODE

03/04/2009

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/798,994	Applicant(s) BECK ET AL.	
	Examiner LUONG T. NGUYEN	Art Unit 2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 16 December 2008.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-5 and 7-14 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-5, 7-14 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1-5, 7-14 filed on 12/16/2008 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1-5, 7-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Borg et al. (US 6,476,864) in view of Hyneczek (US 7,218,350).

Regarding claim 1, Borg et al. discloses an active pixel sensor array sampling system comprising:

a video circuit (column amplifiers 230, figure 3A, column 6, lines 17-60) that generates a video voltage from each pixel in a row of pixels;

a reference circuit (reference column amplifier 240, which generates a unique reference voltage associated with each pixel 10 in each row of active pixel sensor array 280 when the timing controller select which row to read out. It is noted that the reference column amplifier 240 is associated to pixels 10 of active pixel sensor array 280, figure 3A, column 6, lines 17-60) that generates a unique reference voltage associated with each pixel in the row of pixels;

Art Unit: 2622

wherein the video circuit comprises a plurality of video amplifiers (column amplifiers 230, figure 3A, column 6, lines 17-60), each video amplifier being associated with a respective pixel in the row of pixels (each amplifier 230 associated with each pixel 10 on each column line 38, figure 3A, column 6, lines 17-60), the reference circuit comprises a single reference amplifier (reference column amplifier 240, figure 3A, column 6, lines 17-60) associated with all of the pixels in the row of pixels, and the reference amplifier samples the unique reference voltage for each pixel in the row of pixels (column 4, lines 15-29).

Borg et al. fails to specifically disclose the reference circuit that generates a respective unique reference voltage, and the reference amplifier samples the respective unique reference voltage for each pixel in the row of pixels as each pixel in the row of pixels is sampled by a respective one of the plurality of video amplifiers. However, Hyneczek discloses a CMOS image sensor, in which a pulse resets the vertical shift register 306 to make it ready for the new array scan and at the same time causes the reference generator 315 to decrement the reference voltage by one unit step; the reference generator 315 is reset by applying the reset pulse to line 323 (figure 3, column 3, lines 25-67). This indicates that the generator 315 generates a respective unique reference voltage for each pixel 302 in a row of array 301 as each pixel 302 is sampled. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device in Borg et al. by the teaching of Hyneczek in order to provide a practical high performance image sensor that has digital output and high sensitivity (column 2, lines 7-9).

Regarding claim 2, Borg et al. discloses wherein each of the video amplifiers is

Art Unit: 2622

associated with all of the pixels in a respective column of pixels (each amplifier 230 associated with each pixel 10 on each column line 38, figure 3A, column 6, lines 17-60).

Regarding claim 3, Borg et al. and Hyncek disclose a differential amplifier (differential image signal 118, figures 3A, 4, column 6, lines 45-60) that generates a differential voltage responsive to the video voltage and the respective unique reference voltage associated with each pixel in the row of pixels.

Regarding claim 4, Borg et al. discloses the reference amplifier has an output continuously coupled to the differential amplifier during reading of the video voltage of each of the video amplifiers (figures 3A, 4, column 6, lines 17-60).

Regarding claim 5, Borg et al. discloses an active pixel sensor array sampling circuit that samples a voltage on each one of a plurality of pixels, the circuit comprising:

a plurality of video circuits (column amplifiers 230, figure 3A, column 6, lines 17-60), each video circuit generating a video voltage related to a voltage on a respective one of the pixels as its respective pixel is sampled;

a reference circuit (reference column amplifier 240, figure 3A, column 4, lines 15-29, column 6, lines 17-60) that samples a unique reference voltage as each pixel in the plurality of pixels is sampled by the video circuits;

wherein the pixels are arranged in columns and rows, wherein the reference circuit is associated with all of the pixels of each row of pixels, and the reference circuit samples a unique

Art Unit: 2622

reference voltage as each video voltage of each pixel in a row of pixels is sampled (figure 3A, column 4, lines 15-29, column 6, lines 17-60).

Borg et al. fails to specifically disclose the reference circuit that samples a respective unique reference voltage, and the reference circuit samples the respective unique reference voltage as each video voltage of each pixel in a row of pixels is sampled. However, Hyneczek discloses a CMOS image sensor, in which a pulse resets the vertical shift register 306 to make it ready for the new array scan and at the same time causes the reference generator 315 to decrement the reference voltage by one unit step; the reference generator 315 is reset by applying the reset pulse to line 323 (figure 3, column 3, lines 25-67). This indicates that the generator 315 generates a respective unique reference voltage for each pixel 302 in a row of array 301 as each pixel 302 is sampled. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device in Borg et al. by the teaching of Hyneczek in order to provide a practical high performance image sensor that has digital output and high sensitivity (column 2, lines 7-9).

Regarding claim 7, Borg et al. and Hyneczek disclose a differential amplifier (differential image signal 118, figures 3A, 4, column 6, lines 45-60) that provides a differential voltage representing a difference between each sampled video voltage and each sampled respective unique reference voltage.

Regarding claim 8, Borg et al. discloses wherein the reference amplifier has an output

Art Unit: 2622

continuously coupled to the differential amplifier during the sampling of the video voltages for each row of pixels (figures 3A, 4, column 6, lines 17-60).

Regarding claim 9, Borg et al. discloses wherein each video amplifier is associated with all of the pixels of a respective column of pixels (each amplifier 230 associated with each pixel 10 on each column line 38, figure 3A, column 6, lines 17-60).

Regarding claim 10, Borg et al. discloses an integrated circuit including an active pixel sensor array sampling system comprising:

a plurality of video circuits, each video circuit sampling a video voltage from a respective pixel in a row of pixels (column amplifiers 230, figure 3A, column 4, lines 15-29, column 6, lines 17-60);

a reference circuit (reference column amplifier 240, figure 3A, column 4, lines 15-29, column 6, lines 17-60) that samples a unique reference voltage for each pixel in a row of pixels, as each video voltage is sampled by a respective one of the video circuits.

Borg et al. fails to specifically disclose a reference circuit that samples a respective unique reference voltage for each pixel in a row of pixels, as each video voltage is sampled by a respective one of the video circuits. However, Hyncek discloses a CMOS image sensor, in which a pulse resets the vertical shift register 306 to make it ready for the new array scan and at the same time causes the reference generator 315 to decrement the reference voltage by one unit step; the reference generator 315 is reset by applying the reset pulse to line 323 (figure 3, column 3, lines 25-67). This indicates that the generator 315 generates a respective unique reference

Art Unit: 2622

voltage for each pixel 302 in a row of array 301 as each pixel 302 is sampled. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device in Borg et al. by the teaching of Hynecek in order to provide a practical high performance image sensor that has digital output and high sensitivity (column 2, lines 7-9).

Regarding claim 11, Borg et al. discloses a differential amplifier (differential image signal 118, figures 3A, 4, column 6, lines 45-60) that generates a differential voltage responsive to each read video voltage and its respective sampled unique reference voltage.

Regarding claim 12, Borg et al. discloses wherein the pixels are arranged in columns and rows and wherein each video circuit is associated with all of the pixels of a respective column of pixels (figure 3A).

Regarding claims 13 and 14, claims 13 and 14 are method claims of apparatus claims 10-11, respectively. Therefore, claims 13 and 14 are rejected for the reasons given with respect to claims 10-11.

Conclusion

4. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

Art Unit: 2622

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to LUONG T. NGUYEN whose telephone number is (571) 272-7315. The examiner can normally be reached on 7:30AM - 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, DAVID L. OMETZ can be reached on (571) 272-7593. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2622

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/David L. Ometz/
Supervisory Patent Examiner, Art Unit
2622

/L. T. N./
02/26/09